IVY8909B Datasheet

NB-IOT and GSM/GPRS dual mode SOC Processor

Product Specification

Revision1.1.0

1. Product Description

1.1 Overview

IVY8909B is a high performance, highly integrated system-on-chip processor. It could be used as a low power and low BOM cost, NB-IoT and GSM/GPRS application.

IVY8909B integrates all essential electronic components, including baseband, multi-band RF transceiver and a power management unit.

Built around a cost effective 32-bit XCPU RISC core. It offers plenty of processing power for multimedia applications. A high-performance proprietary 16/32-bit digital signal processing engine can further improve overall performance and user experience when performing complex multimedia tasks.

It is also packed with impressive connectivity for easy scalability of the system, allowing glue less interfaces to camera and multimedia companion chips, SDMMC Memory Cards and SPI devices, LCD modules and USB (slave, full speed).

It is GPRS Class 12 enabled, and supports Full Rate (FR), Half Rate (HR), Enhanced Full Rate (EFR) voice coders. It also supports simultaneous dual network operation and integrates a SIM controller with integrated level shifters that can support two SIM cards.

It is available in a small footprint, fine pitch, 8.5 X 9.0 TFBGA package.

1.2Features

- **NB-IoT Communication**
  - 3GPP Release 13 NB-IoT specification fully compliant
  - Software upgradeable to support 3GPP Release 14 features
  - SupportedRFband：1/2/3/4/5/8/12/13/17/18/19/20/25/26/28/66/70/71,wide frequency range
  - Supports all three deployment scenarios (standalone, in-band, and guard-band)
  - Supports both single-tone and multi-tone transmission modes in uplink
  - Supports 200KHz bandwidth in downlink and uplink
  - Supports PSM and eDRX mode
  - Support CP-CIoT and UP-CIoT
  - High mobility supported

- **GSM/GPRS**
  - Dual single-ended LNAs support quad band receiver
  - Fully integrated channel filter
  - High dynamic range ADC
  - Transmitter support quad band
  - Programmable fractional-N synthesizer
  - On die wide range VCO and integrated loop filter
  - Fast settling time suitable for multi-slot GPRS applications
  - Low power mode support 32KHz crystal removal
  - GPRS Class 12
  - Support HR/FR/EFR voice codec

- **Microcontroller subsystem**
  - Up to 192MHz MIPS processor with 16KB I$ and 16KB D$
  - Flexible system frequency at 12/52/72/96/144/192MHz
  - Eight (8) general DMA channels for peripherals and one (1) dedicated channel for debug host
  - One (1) RTC timer with calibration capability
  - Multiple SoC low power modes with rich wakeup sources

- **Memory**
  - Integrated 64Mb SPI NOR Flash

- Integrated 32MbpSRAM
- 64-bit efuse

- **User Interface**
  - Pulse Width Modulator
  - Up to 45 GPIOs with interrupt function
  - Three (3) UART interface
  - One (1) CAM interface
  - One (1) LCD interface
  - 5x5 Keypad interface
  - Two (2) SDIO interface
  - Two (2) I2C interface
  - One (1) USB interface
  - Two (2) GPADC, 10bits

- **Power Management**
  - Complete integrated DC-DC and LDOs solution deriving from VBAT
  - Flexible I/O voltage
  - 5open-drain output switches to supply/control the LED
  - Robust power-on reset (POR) and brown-out reset (BOR)
  - External pin reset

- **Audio**
  - 2channels voice ADC, 8kHz, 13 bits/sample for headset and on-board microphone and line in.
  - Voice DAC, 8kHz, 13 bits/sample for receiver
  - High fidelity Stereo DAC, up to 48kHz, 16 bits per sample for headset
  - Both Class AB and Class D Audio speaker driver

- **ClockSource**
  - 26MHz crystal oscillator
  - 32KHz crystal oscillator or internal 32KHz supplier

- **Debug**
  - Host debug interface allowing non-intrusive in depth investigation
  - GDB debugger
  - Execution logger and profiling through debug port
  - High level text based debugging using Host debug

- **Package**
  - 8.5mm x 9mm, TFBGA package
  - 0.5mm pitch
  - 192balls